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Reg. No. : .....

Name : .....

Fourth Semester B.Tech. Degree Examination, February 2016
(2013 Scheme)
13.402 : COMPUTER ORGANIZATION AND DESIGN (FR)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. a) With examples define various addressing modes of a RISC processor.
   b) If registers R4 and R5 contain decimal numbers 1500 and 4000 respectively, what is the effective address in each of the following cases :
      i) 10(R4) ii) 20(R4, R5).
2. Everything (instruction, data etc.) in a digital computer is stored as 1s and 0s. If you can see the contents of a memory location, can you say whether it is an instruction or data ? How does a computer know whether an item stored in a memory location is instruction or data ?
3. Write the sequence of actions needed to fetch and execute the instruction ***store R6, X (R8)***.
4. a) A PLA unit in a control unit can be considered as a control memory in microprogram control unit, justify.
   b) Explain how PLA program table can be obtained from state table.
5. a) Write the sequence of actions carried out by the processor to handle an interrupt.
   b) What are vectored interrupts ?

PART – B

Answer **one full** question from **each** Module, **each full** question carries **20** marks.

Module – I

6. a) Explain how nested subroutines are handled by the processor. **10**
   b) Discuss the logic, shift and rotation instructions of a RISC processor. **10**

P.T.O.

7. a) The immediate and absolute modes in a RISC – style processor restrict the operand size to 16 bits. How does a RISC processor handle a 32-bit value ? 8

   b) Draw a schematic diagram of interface used for keyboard and display. Explain the registers of the interface. What are the different methods used for I/O transfer ? 12

Module – II

8. a) How different addressing modes (absolute, indirect and index) for load and store instruction can be obtained by implementing only index mode ? 6

   b) Draw the block diagram for the hardware implementation of the following register Transfer : $x'T_1 : A \leftarrow B$. 6

   c) Illustrate a bus system for a processor with four registers R_0, R_1, R_2 and R_3, two multiplexers for source registers and a decoder for destination. What are values of select lines for the following operation : Add R_0, R_1, R_2. 8

9. Design an Accumulator with the capability to perform the following microoperations : Add, Clear, Complement, AND, OR, EX-OR, Shift right, Shift left and Increment. 20

Module – III

10. Design a hardwired control unit to perform addition and subtraction of two binary numbers represented in sign-magnitude form. The final result must be in sign-magnitude form. 20

11. a) What are the essential address sequencing capabilities of typical sequencer ? 8

    b) With a schematic diagram explain organization of a typical microprogram sequencer. 12

Module – IV

12. a) Explain internal organization of bit cells in a memory chip with bit line, word line and sense/write circuit. 12

    b) Compare static and dynamic RAMs. 8

13. a) Explain data transfer technique using DMA. 8

    b) Explain the concept of set-associative mapping. 12